MITE – A Bit Serial Single Board Computer.  
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**Introduction.**  
  
Before the introduction of the microprocessor, it was common to build minicomputers and mainframes using discrete TTL ICs. Some examples are the Data General Nova, the PDP-11 and the PDP-8/I, all appearing around 1969, 1970. At the same time, electronic desktop calculators were being commercialised, and many of these used bit-serial arithmetic, to keep the component cost to a minimum.  
  
Bit serial arithmetic is usually based around a serial adder. It processes the operands a pair of bits at a time, producing the sum of the bits and any carry generated that is then stored in a flipflop and included in the sum of the next pair of bits.  
  
Arithmetic starts with the least significant pair of bits, for example AC0 and B0. AC is the accumulator and B is a shift register connected to the memory bus. After loading the B register from the bus, data is shifted through the ALU, and at the end of the operation, the result is held in the accumulator. From there, the result can be written back to memory.  
  
The bit serial ALU can be extended to include subtraction, inversion, negation and the common Boolean logic operations AND, OR, XOR and there inverted forms.  
  
The ALU is just 5 simple 74HC series ICs. No additional ICs are needed, even if the wordsize is increased from 8, to 16, or 32 bits.  
  
**Technical Description.**MITE can be broken down into several sub-systems for clarification of its operation.  
  
1. A clock generator and timing sequencer

2. A Program Counter and SRAM memory Interface  
3. Instruction decoding logic

4. An Accumulator shift register AC

5. A memory Bus shift register B

6. The bit serial ALU

7. Input and Output registers

**Clock Generator and Timing Sequencer.**A 74HC4060 14-stage counter and crystal oscillator provides the means to generate a clock signal from KHz to MHz. The various clock frequencies are link selectable.  
  
A 74HC4017, decoded, decade counter provides 10 decoded timing slots T0 to T9. These timing signals are used to coordinate all of the operations of the MITE computer.  
  
In brief:  
  
T0:   
  
The 8-bit instruction and its accompanying payload data byte are fetched from SRAM and latched. The B register is loaded from the memory bus.  
  
T1 to T8:

8 clock pulses clock the data from the B register, through the ALU and into the AC register.  
  
T9:

The result of the ALU operation is written back to memory.  
  
In a 16-bit system, two timing states S0 and S1 are generated. S0 handles the low byte from memory, S1 deals with the high byte. A complete 16-bit operation is accomplished in 20 timing pulses.  
  
**Program Counter and parallel SRAM Interface.**This is by far the most complex sub-system of the MITE computer.   
  
The Program Counter consists of four 74HC161, 4-bit counters, ganged together to generate a 16-bit address.  
  
The memory can be a 62256 32Kx8 SRAM, 28C256 EEPROM, a 128Kx8 SRAM or a mix of SRAM and EEPROM.  
  
Instructions are stored at even addresses (A0=0) and the payload databyte is stored at the next address PC+1 (A0=1).  
  
On the transition to T1, both the instruction and the payload databyte are held in 74HC574 8-bit registers and will be retained there until the next T0.  
  
The payload databyte is loaded into the B shift register during T1 and will then be clocked through the ALU during T states T1 to T8.  
  
The databyte may be an 8-bit literal to be used in logic or arithmetic operations, or an 8-bit address, within the current page, or an 8-bit jump address. It may also be used to provide further ALU operations, when memory is not being referenced.  
  
**Instruction Decoding Logic.**

Once the instruction word is held in the 74HC574 instruction register, it is decoded using combinational logic to control the operation of the ALU. The decoding is done using a 74HC138, 3 to 8 line decoder, a diode array and a 74HC540 octal inverter.  
  
The decoded lines directly control the operation of the ALU allowing 8 basic instructions to be performed.  
  
**Accumulator Shift Register.**  
  
This is a 74HC595 serial in -parallel out 8-bit shift register . It has a tristate output bus so that it can directly interface to the memory bus. It holds the result of the ALU operation, which can be written to memory during T-state T9.  
  
**Bus Register B.**  
The B register is a parallel loaded 8-bit shift register, type 74HC165. Its primary purpose is to convert parallel data from the memory bus into a serial bitstream, so that it can be processed by the bit serial ALU, and then onto the Accumulator.  
  
It is loaded with the payload databyte during T0. It then clocks this data out between T1 and T8, through the ALU and into the Accumulator.  
  
**Bit Serial ALU.**  
  
This consists of a full-adder, a multiplexer, and a 74HC74 D-type flipflop to hold the interim carry and make it available for the next pair of bits arithmetic operation.  
  
The full adder consists of a 74HC86 quad 2-input XOR gate and a 74HC00 quad 2-input NAND gate. Two of the XOR gates are used to selectively invert the A or B inputs, allowing subtraction, inversion and negation.  
  
A full adder generates the Boolean sum of the An and Bn bits – this is *An XOR Bn*.  
  
It also generates a carry - which is *An AND Bn*.  
  
The multiplexer can select between *An XOR Bn* and *An AND Bn* to provide these two logic functions for free.  
  
Selecting both *An XOR Bn* and *An AND Bn* gives the Boolean OR *An OR Bn*.  
  
Selecting neither, gives logic zero – which is a convenient way of clearing the Accumulator.  
  
**Input and Output Registers.**  
  
MITE is intended to interface with SPI peripherals. The result in the Accumulator can be output as a standard SPI packet. Similarly, a SPI packet can be received and loaded into memory.  
  
  
**Construction.**  
  
The 8-bit MITE is 25 ICs, the 16-bit version is fewer than 30 ICs.